

Luo Qin

Male, Birthday Day: 31/Dec/1996, Born in: Hunan, China
Address: Rm C315, Jockey Club Postgraduate Hall 1, The Chinese University of Hong Kong,
Shatin, New Territories, Hong Kong SAR
TEL: +85267329754 Email: qluo22@cse.cuhk.edu.hk

Education Background

- **2022-Present** **Ph.D student** **The Chinese University of Hong Kong**
Computer Science and Engineering **Supervisor:** Evangeline FY Young
Research topics: Optimization of the FPGA prototyping flow, Machine Learning in EDA
- **2019-2022** **Master** **Shanghai Jiao Tong University**
Automation **Supervisor:** Xiaolin Huang
Research topics: Acceleration in Kernel Methods and Neural Networks
- **2015-2019** **Bachelor** **Shanghai Jiao Tong University**
Instrument Science and Engineering

Publication

[1] **Qin Luo**, Xinshi Zang, Qijing Wang, Fangzhou Wang, Evangeline F.Y. Young, Martin D.F. Wong. A Routability-Driven Ultrascale FPGA Macro Placer with Complex Design Constraints. 2024 IEEE 32nd Annual International Symposium on Field-Programmable Custom Computing Machines (FCCM). (Short Paper), 2024.

[2] **Qin Luo**, Kun Fang, Jie Yang, Xiaolin Huang. Towards Unbiased Random Features with Lower Variance For Stationary Indefinite Kernels. International Joint Conference on Neural Networks (IJCNN), 2021.

[3] Tianshu Chu, **Qin Luo**, Jie Yang, Xiaolin Huang. Mixed-precision Quantized Neural Networks with Progressively Decreasing Bitwidth. Pattern Recognition (PR), 2021, 111: 107647.

Internship

- **2020.12.01-2021.01.30** **Megvii-Shanghai Research Institute** **Algorithm Intern**
Supervisor: Yuke Zhu, Yichen Wei
-Assist the algorithm engineer to solve the problems in the implementation of the algorithm.
-Development of the action recognition badcase analysis system.
-Exploration to speed up the Transformer Model.

Award

Third Place, MLCAD 2023 contest, FPGA Macro Placement

Third Prize, Simultaneously Dynamic Networking and Circuit Partitioning, Integrated Circuit EDA Elite Challenge, 2022

Third Place, ISPD 2023 contest, Advanced Security Closure of Physical Layouts

Second Place, FPGA 2024 contest, Runtime-First FPGA Interchange Routing Contest

Outstanding Graduate in Shanghai Jiao Tong University, 2019 & 2022.

Service

Reviewer of Design Automation Conference (DAC), IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Expert Systems With Applications, IEEE Transactions on Neural Networks and Learning Systems (TNNLS)